

Amendments to the Specification:

Please replace the paragraph that begins on page 11, line 6, with the following paragraph:

In normal operation, the output of flip-flop 72 will be high half of the time, holding the gate of transistors QFR high at least half of the time through OR gates 62 and 82. Whenever the gate of transistor QFR is low, the combination of resistor Rff and capacitor Cff (see Figure 1) will generate a ramp which is connected to the VRAMP which is compared with the feedback voltage Vf by comparator 84. When the ramp voltage exceeds the feedback voltage, the output of OR gate 64 will go high, setting RS flip-flop 86 to drive the Q output of flip-flop 86 high, and thus the output of NOR gate 74 low, to turn off highside and lowside switches (switching transistors) QH and QL. Thus, the highside and lowside switches are off at least 50% per of the time, and such additional time as required to maintain the desired output voltage, as characteristic of pulse width modulated switching regulators. Also, the current through the sense resistor RS connected to the drain of transistor Qhs is sensed by amplifier 58 to provide a voltage IOUT proportional to the current. Also, if the current ever exceeds a predetermined limit, then the output of comparator will go high, setting RS flip-flop 86 through OR gate 64 to drive the Q output of flip-flop 86 high, and thus the output of NOR gate 74 low, to turn off the highside and lowside switches QH and QL for the rest of that clock cycle. Thus the circuit limits the rate of increase of voltage on the input to the pulse width modulator or other power integrated circuit powered by the soft start circuitry, or the maximum current provided to that integrated circuit, whichever reaches its predetermined limit first. In the circuit shown in Figure 3a, current Ib0 aids in the generation of the ramp, with resistor Rff providing feed forward of the input voltage to the regulator for immediate reduction in the pulse width upon increase of the input voltage, and vice versa. Also, the switching of the highside switch QH and the resulting voltage variation in the highside transformer terminal XFRMRH, together with the diode DBST, charge the boost capacitor Cb (see Figure 1) to provide increased gate drive for the highside transistor. Also during normal operation, the Global Shutdown signal is low, holding transistor QSS off and allowing the current source ISS to maintain a charge on capacitor C_{ss} (Figure 1).